~~What is claimed is:~~

1. An arrangement having p-doped semiconductor layers (12, 20, 22) and n-doped semiconductor layers (14, 10) which exhibits transitions between the p-doped semiconductor layers (12, 20, 22) and n-doped semiconductor layers (14, 10), the transitions displaying a Zener breakdown upon application of a voltage characteristic of a transition, wherein a plurality of transitions between p-doped semiconductor layers (12, 20, 22) and n-doped semiconductor layers (14, 10) are present; and the characteristic voltages additively make up the breakdown voltage of the entire arrangement.

2. The arrangement as defined in Claim 1, wherein the semiconductor layers (10, 12, 14, 20, 22) are highly doped.

3. The arrangement as defined in Claim 1 or 2, wherein the semiconductor layers (10, 12, 14, 20) exhibit constant doping.

4. The arrangement as defined in one of the foregoing claims, wherein the p-doped semiconductor layers (12) and n-doped semiconductor layers (14) are doped at the same concentration.

5. The arrangement as defined in one of the foregoing claims, wherein the p-doped semiconductor layers (20, 22) form at least two groups that are doped at different concentrations.

6. The arrangement as defined in one of the foregoing claims, wherein the n-doped semiconductor layers form at least two groups that are doped at different concentrations.

7. The arrangement as defined in one of the foregoing claims,
wherein the semiconductor layers (12, 14, 20, 22) are arranged on an n-doped substrate (10).

8. The arrangement as defined in one of the foregoing claims,
wherein the semiconductor layers are arranged on a p-doped substrate.

9. The arrangement as defined in one of the foregoing claims,
wherein the doping type of the semiconductor layer farthest away from the substrate (10) corresponds to the doping type of the substrate (10).

10. The arrangement as defined in one of the foregoing claims,
wherein the doping type of the semiconductor layer farthest away from the substrate is different from the doping type of the substrate.

11. The arrangement as defined in one of the foregoing claims,
wherein the semiconductor layers (12, 14, 20, 22) have a thickness of approximately 4 µm.

12. The arrangement as defined in one of the foregoing claims,
wherein the substrate (10) has a thickness of approximately 500 µm.

13. The arrangement as defined in one of the foregoing claims,
wherein the doping concentration is in the region of 2 x 10^{19} atoms/cm^3.

14. The arrangement as defined in one of the foregoing claims,
wherein approximately ten transitions between p-doped semiconductor layers (12) and n-doped semiconductor layers (14) are provided.

15. The arrangement as defined in one of the foregoing claims,
wherein it has on its upper side and lower side respective metal contacts (16, 18) which extend over their entire surface.

16. The arrangement as defined in one of the foregoing claims,
wherein the semiconductor layers (10, 12, 20, 22) are silicon layers.

17. A method for manufacturing an arrangement having p-doped semiconductor layers (12, 20, 22) and n-doped semiconductor layers (14, 10) which exhibits transitions between the p-doped semiconductor layers (12, 20, 22) and n-doped semiconductor layers (14, 10), the transitions displaying a Zener breakdown upon application of a voltage characteristic of a transition, a plurality of transitions between p-doped semiconductor layers (12, 20, 22) and n-doped semiconductor layers (14, 10) being present, and the characteristic voltages additively making up the breakdown voltage of the entire arrangement, the method comprising application of the semiconductor layers (12, 14, 20, 22) by epitaxy.

18. The method as defined in Claim 17,
wherein the epitaxy takes place at approximately 1180°C.

19. The method as defined in Claim 17 or 18,
wherein the epitaxy is performed at a growth rate of approximately 4 µm/min.

20. The method as defined in one of Claims 17 through 19, wherein metal contacts (16, 18) are sputtered onto the upper side and lower side of the arrangement.

21. The method as defined in one of Claims 17 through 20, wherein the arrangement is divided into individual chips after the metal contacts (16, 18) are sputtered on.

22. The method as defined in one of Claims 17 through 21, wherein the edges of the chips are removed.

23. The method as defined in one of Claims 17 through 22, wherein thin silicon disks are assembled by wafer bonding.